REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed January 12, 2004. Reconsideration and allowance of the application and pending claims 1-16 are respectfully requested.

I. Drawings Objections

The drawings have been objected to under 37 C.F.R. 1.84 as described on the PTO-948 form. In response to this objection, the drawings have been amended to address the informalities noted in the form. A clean copy of Figures 1-11 and a marked-up copy of Figures 1-11 that shows all changes in red ink have been included with this Response. It is asserted that no new matter has been added.

II. Claim Rejections - 35 U.S.C. § 112

A. Rejections under 35 U.S.C. § 112, Second Paragraph

Claims 1-16 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. In particular, the Office Action alleges the following:

> The preamble of claim 1 states, "A method for testing circuits having analog components..." however there is no reference in the body of claim 1 to the analog components. Claim 4 cites "The method of claim 1, wherein the low-cost optimized test is designed to maximize the sensitivity of the circuit response to changes in circuit process parameters" which cites an intention of use but does not particularly point out the design of the test that achieves this maximized sensitivity of the circuit response. Claim 7, cites "..wherein the optimized test is created such that the number of

specification based tests needed is minimized" which cites an intention of use but does not particularly point out how the optimized test is created so as to achieve the minimization of the number of specification based tests. Claim 9, line 2, cites "the specifications" however the antecedent basis is "one or more predetermined circuit specifications". Claim 10, line 2, cites "the measurement response", however the antecedent basis is "circuit response". Claim 12, line 2, cites "the various circuit specifications" however the antecedent basis is "predetermined specifications".

In response to these rejections, Applicant has amended according to the suggestions indicated above, except for claim 10 as noted. In addition to the above noted amendments, various other changes have been made to the claims to provide an accurate and precise description of Applicant's originally disclosed invention.

In view of the above described amendments to the claims, it is respectfully asserted that claims 1-16 currently define the invention in the manner required by 35 U.S.C. § 112. Accordingly, it is respectfully requested that the rejections to these claims be withdrawn.

III. Claim Rejections - 35 U.S.C. § 103(a)

A. Rejection of Claims

1. Statement of the Rejection

Claims 1, 2, 8, 10-12 and 15 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Bhattacharya, et al.* ("*Bhattacharya*", U.S. Pat. No. 5,748,647) in view of *Dahbura, et al.* ("*Dahbura*", U.S. Pat. No. 4,991,476) and *Balzer* ("*Balzer*", U.S. Pat. No. 5,327,437).

Applicant respectfully traverses this rejection.

B. Applicant's Claimed Invention

1. A method for testing circuits having **analog components**, comprising:

performing a low-cost optimized test on the circuit by applying an optimized input stimulus to the circuit, **the circuit having analog components**;

capturing the circuit response to the input stimulus applied to the **circuit**;

evaluating the circuit response to predict whether the performance parameters of the circuit satisfies predetermined specifications for the circuit; and

making a pass/fail determination for the **circuit** based upon the evaluation of the circuit response.

C. Discussion of the Rejection

As acknowledged by the Court of Appeals for the Federal Circuit, the U.S. Patent and Trademark Office ("USPTO") has the burden under section 103 to establish a proper case of obviousness by showing some objective teaching in the prior art or generally available knowledge of one of ordinary skill in the art that would lead that individual to the claimed invention. See *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Accordingly, to make a proper case for obviousness, there must be some prior art teaching or established knowledge that would suggest to a person having ordinary skill in the pertinent art to fill the voids apparent in the applied reference. It is respectfully asserted that no such case has been made in the outstanding Office Action.

In addition to the above described defects of the rejection, Applicant respectfully asserts that the proposed combination is improper. It has been well established that teachings of references can be combined only if there is some suggestion or incentive to do so. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, there must be a teaching in the relevant art which would suggest to a person having ordinary skill in that art the desirability of the claimed

invention. It is respectfully asserted that no such case has been made in the outstanding Office Action.

The Office Action alleges the following:

> As per claim 1, Bhattacharya et al. (Abstract, col. 9 lines 31-40, col. 13 lines 59-62) disclose "capturing the circuit response to the input stimulus applied to the circuit." Bhattacharya et al. (Abstract, col. 2 lines 27-33, col. 3 lines 43-46, col. 7 lines 56-67, col. 8 lines 1-49, col. 10 lines 36, 37 and Tables 1, 4 and 5) disclose "evaluating the circuit response to predict...satisfies predetermined specifications for the circuit." It appears though that Bhattacharya et al. does not clearly disclose the performing and making steps. However, Dahbura et al. (Abstract, col. 2 lines 18-30, col. 4 lines 20-30) teach "performing a low-cost optimized test...by applying an optimized input stimulus to the circuit." It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Dahbura et al. to the invention of Bhattacharya et al. as specified above because as taught by Dahbura et al. (Abstract) every testable aspect of the entity is guaranteed to be tested using a minimum number of steps which represents a considerable cost savings. It appear though that the above combination of references still does not clearly teach the making step. However, Balzer (see at least abstract) teaches "making a pass/fail determination for the circuit based upon the evaluation of the circuit response." It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply the techniques of Balzer to the inventions of Bhattacharya et al. and Dahbura et al. as specified above because as taught by Balzer (Abstract, col. 1 lines 28-40) measurement noise may result in an actual parameter value that falls outside of an acceptable range but due to noise, the measured value of that parameter may be inside the acceptable range, thereby causing the tested device to be erroneously accepted and alternatively, an actual parameter value may fall within the acceptable range, but due to noise the measured value of the parameter may be outside of the acceptable range, thereby causing the tested device to be erroneously rejected. The techniques of Balzer would resolve the above measurement noise problem providing a method for testing which is operable in the presence of measurement noise.

With respect to independent claim 1, the references do not disclose, teach, or suggest all of the claim limitations, either alone or in combination. Initially, *Bhattacharya* does not disclose capturing and evaluating steps for a circuit having analog components. *Bhattacharya* discloses systems and methods for RT-level specifications, which is understood in the art to comprise digital components. Thus, the amended claim limitation (initially provided for in the preamble of claim 1) that provides that the **circuit** upon which the capturing and evaluating steps occurs includes **analog components** is not met by *Bhattacharya*.

Further, Applicant respectfully submits that the deficiencies noted above are not remedied by the use of *Dahbura*. *Dahbura* provides for, as indicated in the title, optimal test generation for **finite state machine models** (emphasis added). By definition, finite state machine models would be understood in the art as not representing circuits that include analog components, as analog is generally understood as representing a continuum of data. Thus, neither *Bhattacharya* nor *Dahbura*, alone or in combination, disclose, teach, or suggest a method of evaluating, capturing, and performing on circuits that include **analog components** as recited in claim 1.

Further, Applicant respectfully submit that there is no suggestion to combine *Bhattacharya* and *Dahbura*. *Bhattacharya* seeks to minimize full scan testing (see column 1), where in contrast, *Dahbura* uses exhaustive testing (see Abstract). The suggestion or motivation to combine these two references is neither explicit, nor inherent, as apparently they operate in a dissimilar manner.

Balzer does not explicitly disclose that the **circuit** under test includes **analog components**, and thus fails to meet all of the claim limitations recited in claim 1.

Regarding the use of *Balzer* in combination with *Bhattacharya* and *Dahbura*, Applicant fails to see the suggestion or motivation to combine *Balzer* with either *Bhattacharya* and *Dahbur*. *Balzer* discloses an iterative method to address noise in testing. *Bhattacharya* seeks to minimize full scan testing and *Dahbura* uses exhaustive testing. Not only do these references address distinct problems, but nowhere is it evident in either of these references the motivation or suggestion to combine these references.

Thus, since neither *Bhattacharya*, *Dahbura,* nor *Balzer*, alone or in combination, disclose, teach, or suggest all of the claim limitations of claim 1, and since there is no motivation or suggestion to combine the aforementioned references, Applicant respectfully requests that the rejection to claim 1 be withdrawn.

Because independent claim 1 is allowable over the cited references, dependent claims 2-16 are allowable as a matter of law for at least the reason that the dependent claims 2-16 contain all of the elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

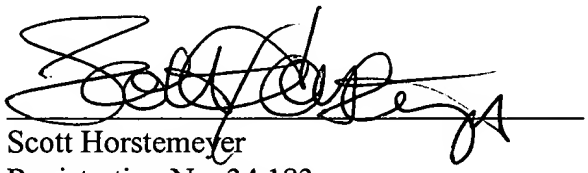
In addition, Applicant also respectfully requests that the next Office Action address dependent claims 3-7, 9, and 13, as the patentability of these claims were apparently not addressed in the last Office Action.

In summary, it is Applicant's position that a proper case for obviousness has not been made against Applicant's independent claim 1 and claims 2-16 which depend therefrom. Therefore, it is respectfully submitted that each of these claims is patentable over the cited references and that the rejection of these claims should be withdrawn.

CONCLUSION

Applicant respectfully submits that pending claims 1-16 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, Virginia 22313-1450, on 4-12-04.

Mary Meegan
Signature

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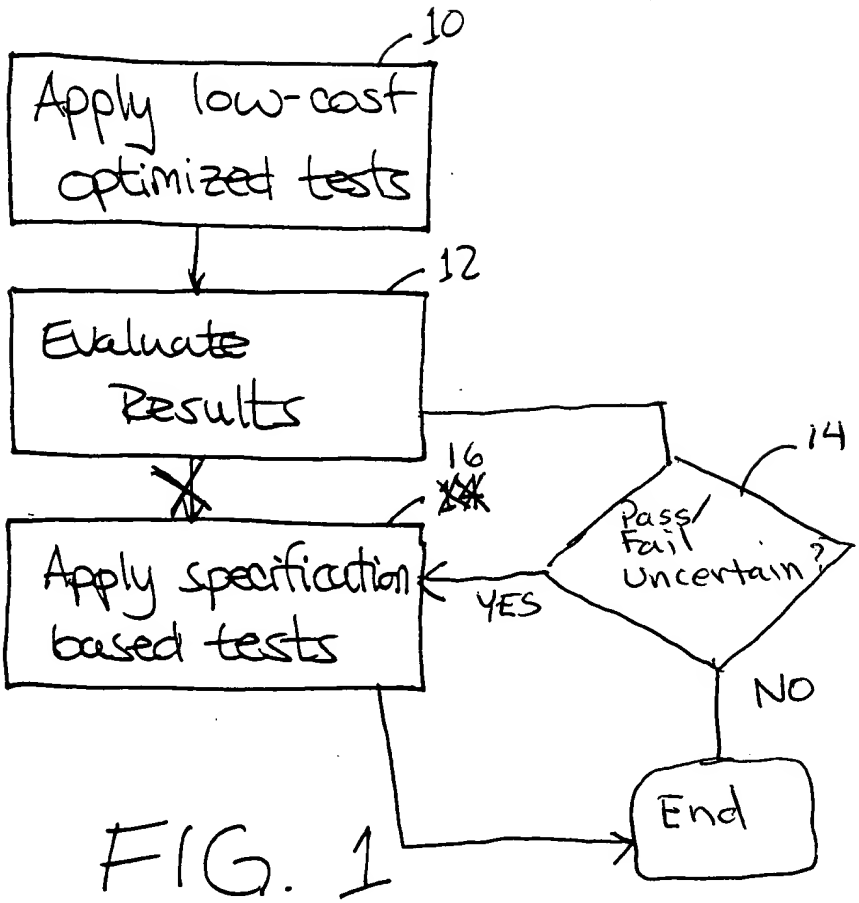

FIG. 1

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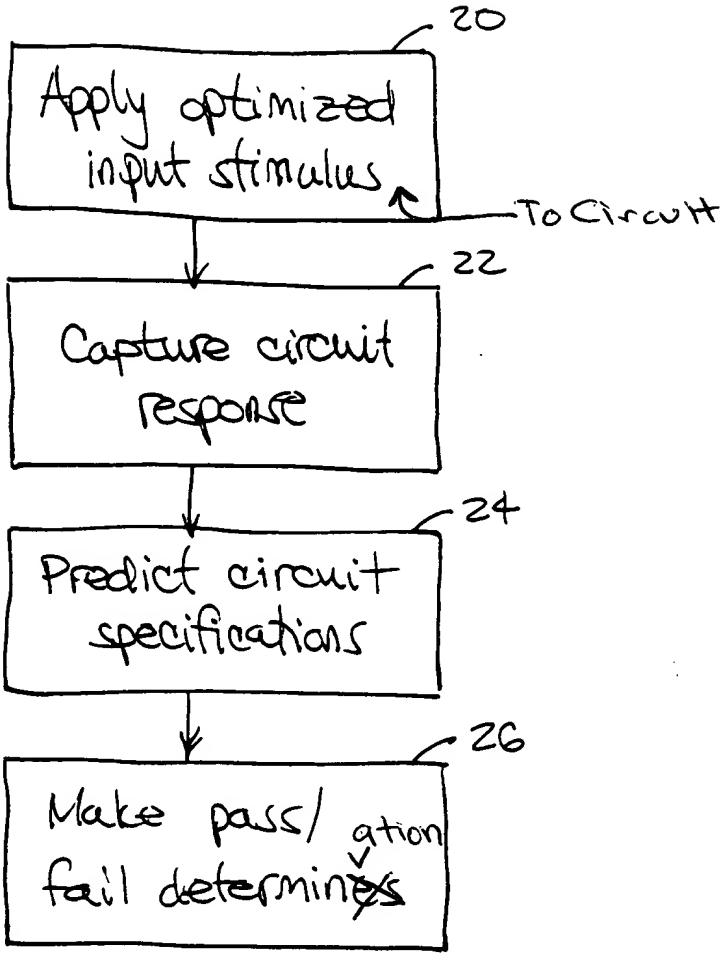

FIG. 2

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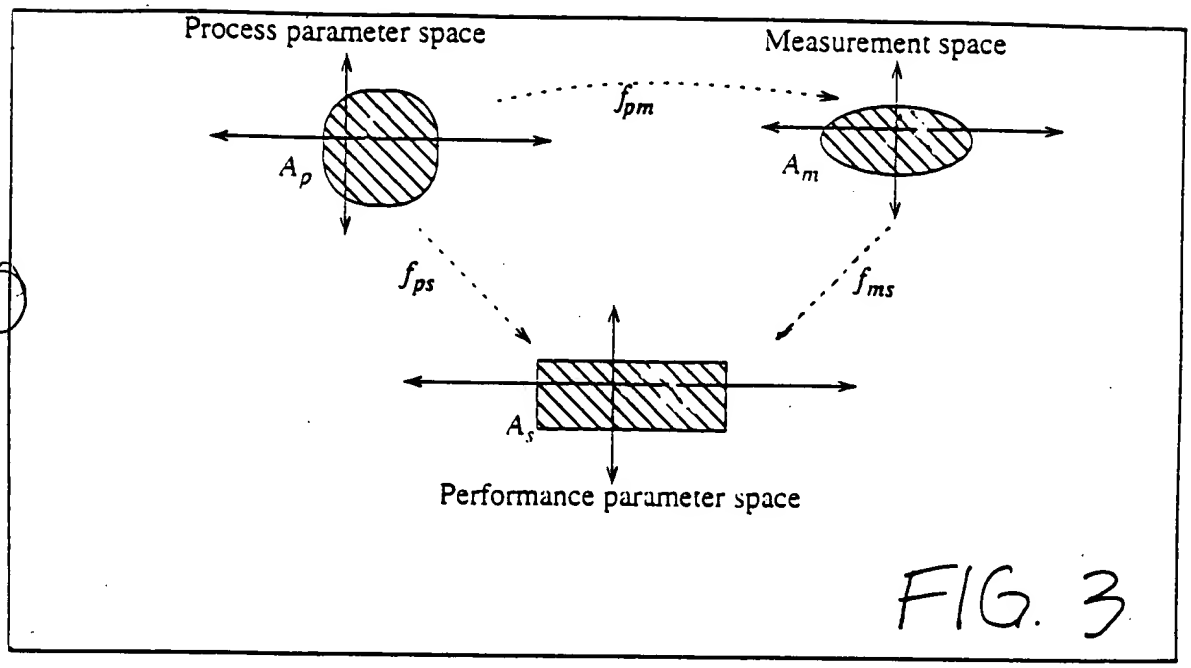

FIG. 3

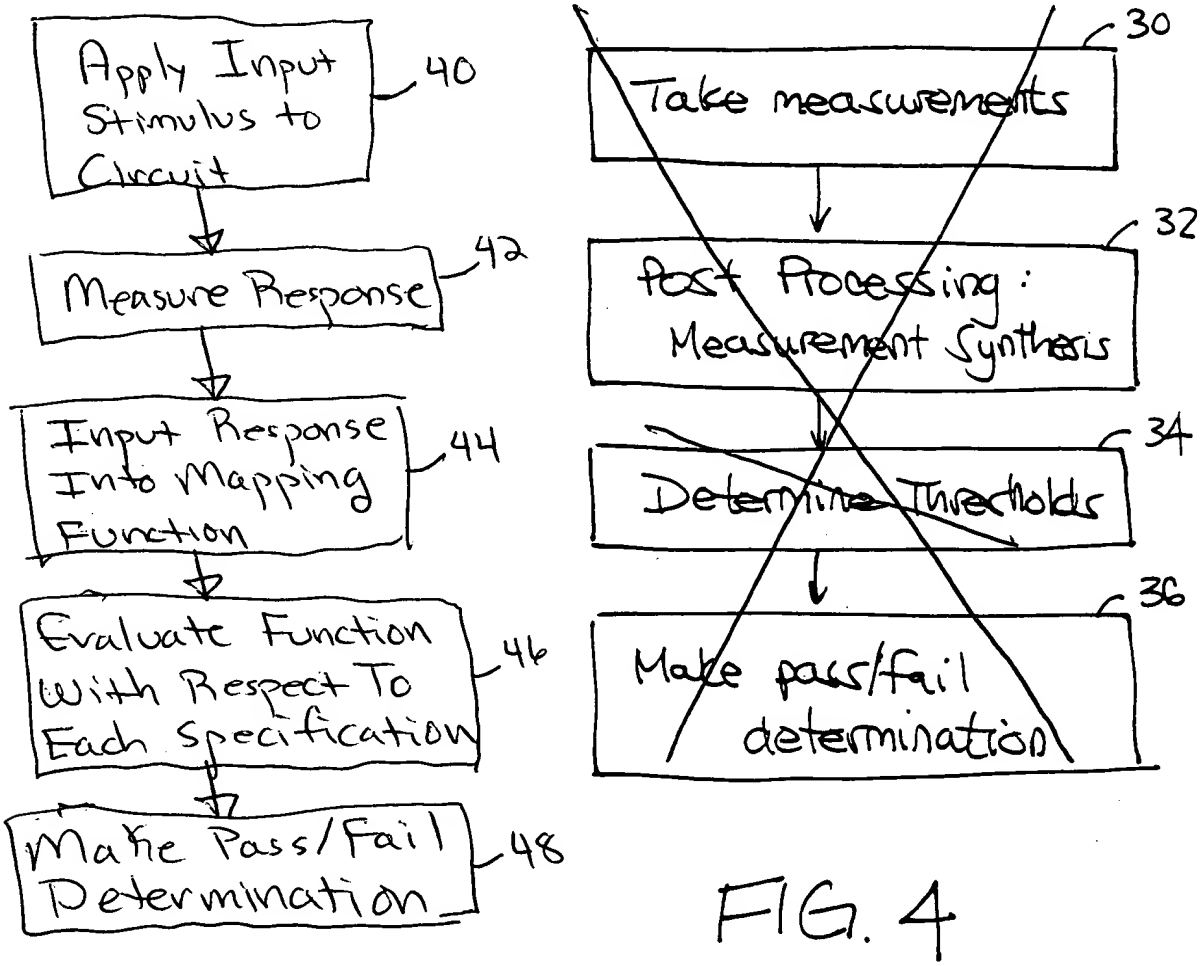

FIG. 4

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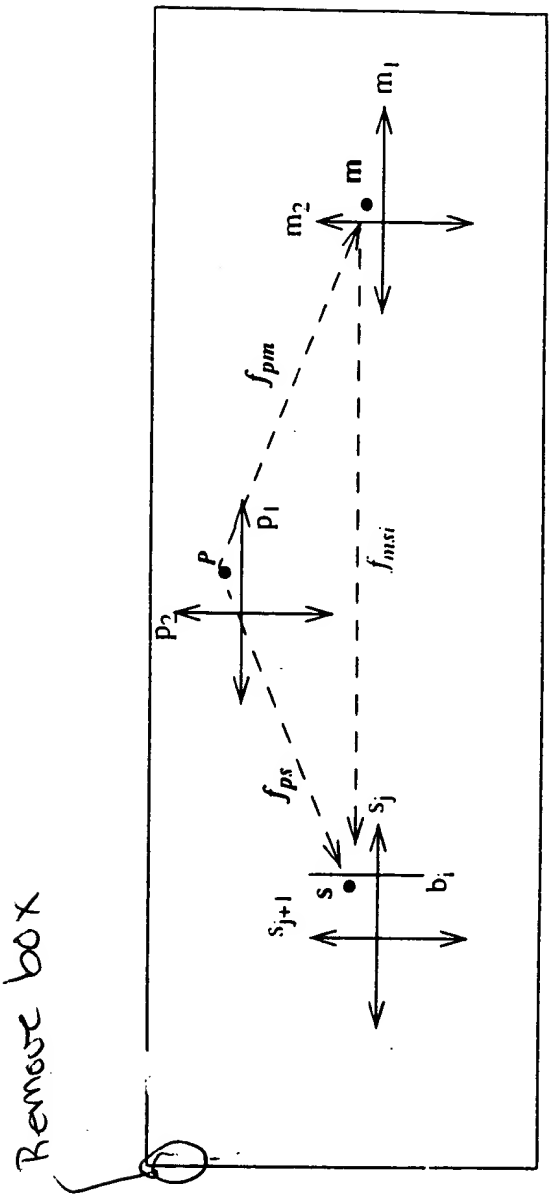

FIG. 5

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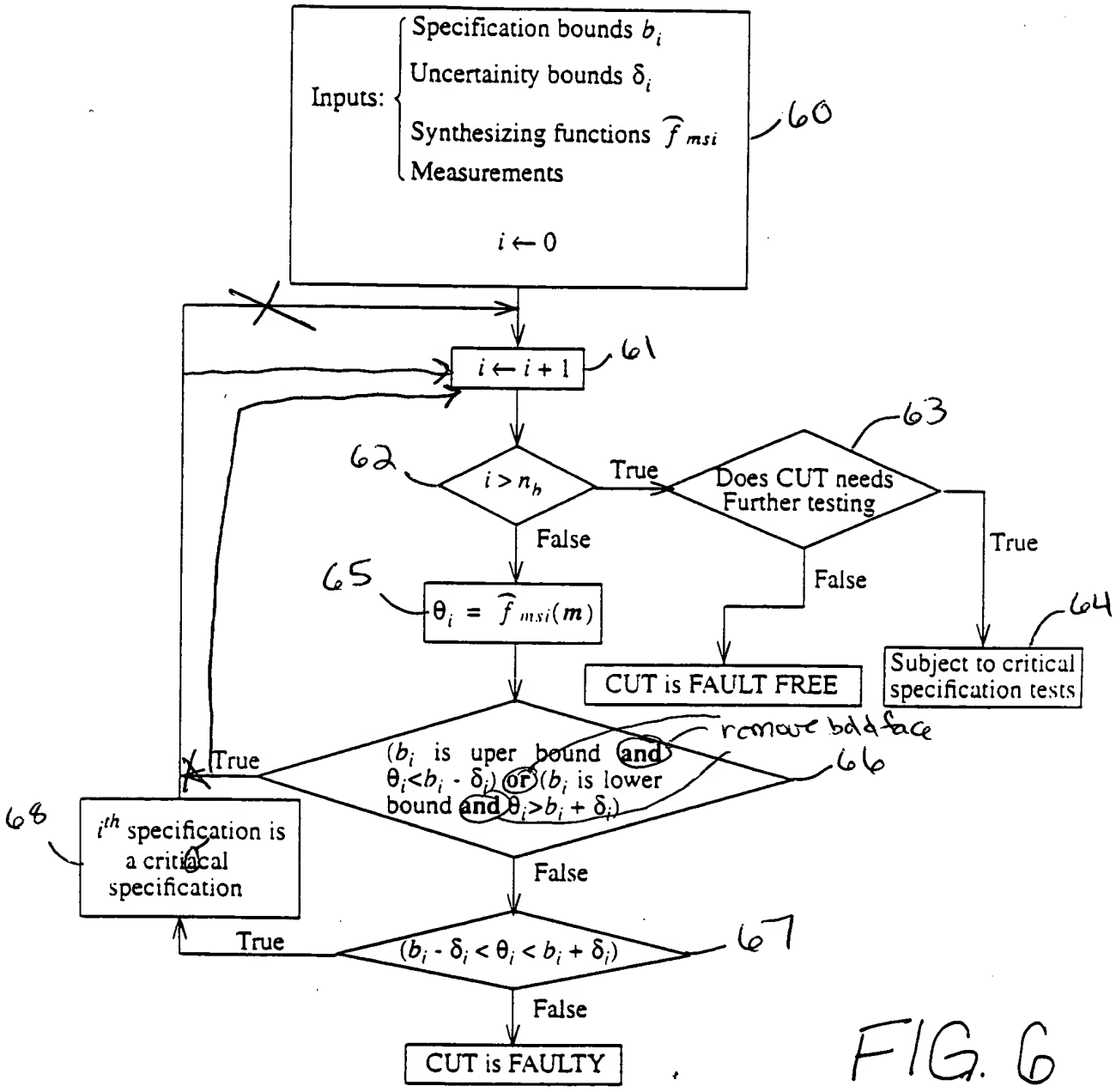

FIG. 6

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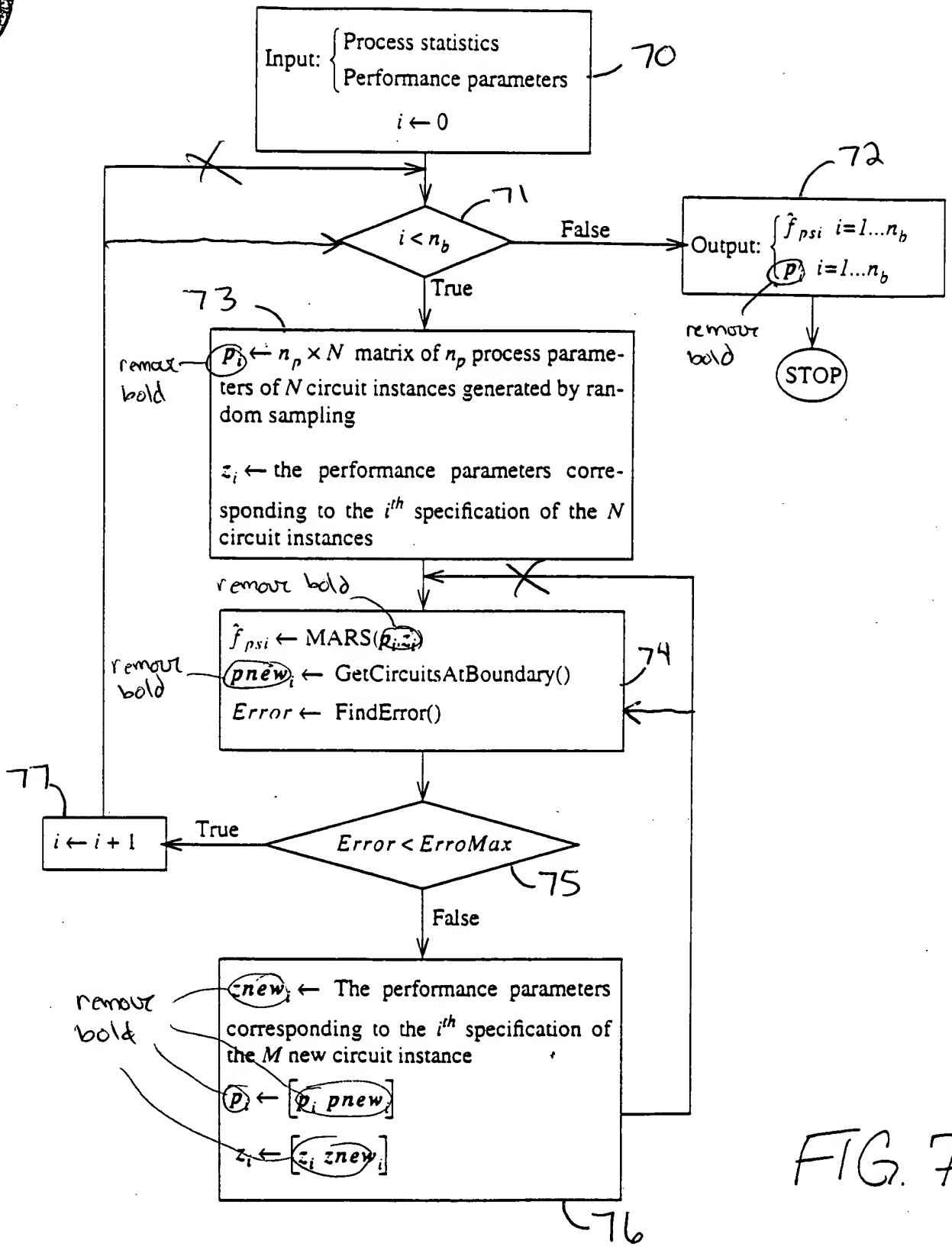

FIG. 7

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Procedure OrderMeasurements
01 **for** each i^{th} single ended specification
02 **for** each measurement
03 remove the measurement from the list of independent variable
04 derive the synthesizing function using MARS. Use the training set generated by GenerateTrainSet to train MARS
05 Calculate the variance σ_{ei}^2.
06 **end for**
07 Order the measurements in the acending order of σ_{ei}^2.
08 **end for**

Procedure SelectMeasurements
01 **for** each single ended specification
02 Selected measurements = Φ
03 **repeat**
04 Add the measurement with lowest σ_{ei}^2 to the set of selected measurements.
Use the ordered list of measurements generated by OrderMeasurements
05 Derive the synthesizing function with the selected set of measurements
06 Calculate the variance σ_{ei}^2
07 **until** σ_{ei}^2 start increasing.
08 **end for**

FIG. 8

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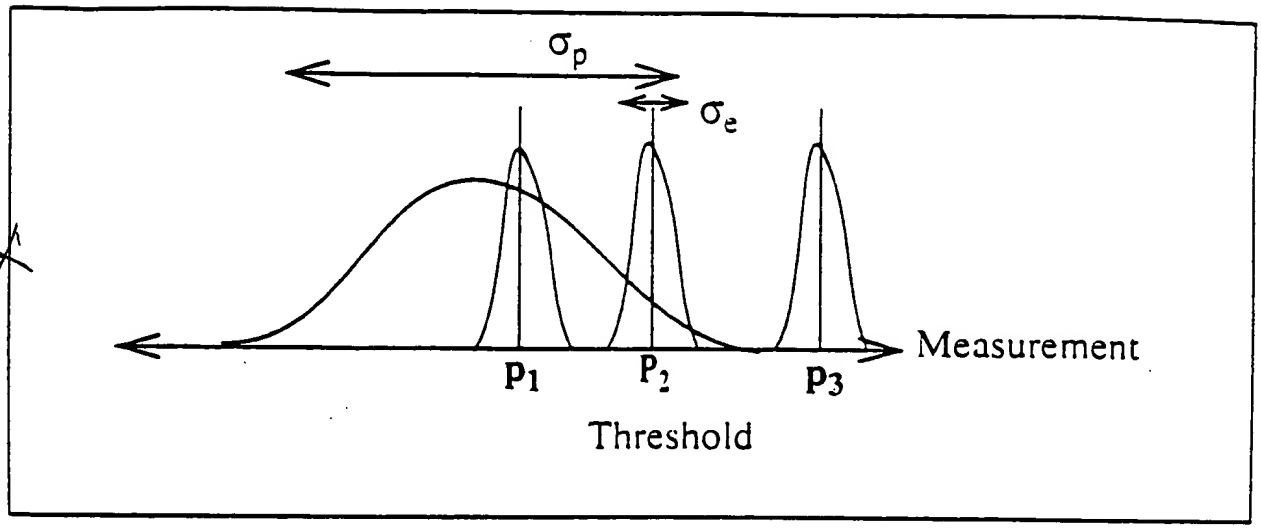

FIG. 9

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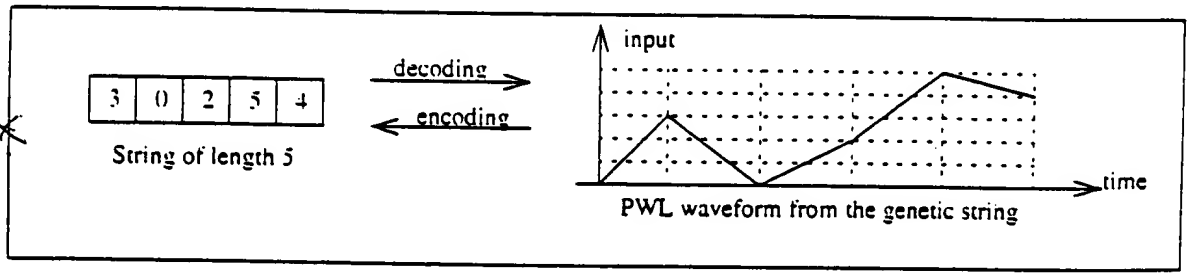

FIG. 10

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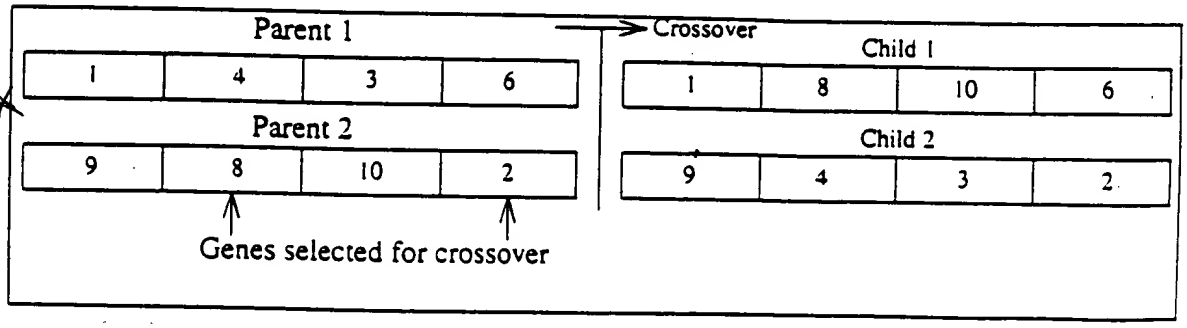

FIG. 11